

REMARKS

In view of the amendments proposed above, Applicants respectfully request consideration of the following remarks.

Drawing Objection

The Examiner has objected to FIG. 1, stating that this figure "should be designated by a legend such as – Prior Art – because only that which is old is illustrated." Office Action, at page 2. Applicants submit herewith a replacement sheet for FIG. 1, wherein this figure has now been labeled "Prior Art", as suggested by the Examiner.

Applicants also submit herewith a replacement sheet for FIG. 3. In the replacement figure, the reference numeral 305 has been added, which was inadvertently omitted from the as-filed FIG. 3.

Anticipation Rejections Under 35 U.S.C. § 102

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Anticipation Rejection Based on United States Patent Application Publication US

2002/0199052 to Moyer

Claims 1-29 were rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent Application Publication 2002/0199052 to Moyer (hereinafter "Moyer"). Applicants respectfully traverse this rejection as set forth below.

Moyer discloses a bus arbitration scheme for the global bus of a computer system that includes – in addition to the global bus (see FIG. 1, item 12) – a CPU 14, system memory 20, 22, 24, alternate bus masters 36, 38, 40, peripherals 28, 30, and a bus arbiter 34, all coupled with the global bus 12. Moyer, at paragraphs 0017 and 0022 (lines 1-3). The bus arbiter 34 includes (see FIG. 4) a Logic Circuit 50 coupled with the global bus 12 to receive Current Transfer Type Signals 53. Moyer, at paragraph 0021. Bus arbiter 34 also includes a Policy Select Logic circuit 54 coupled with Logic Circuit 50, wherein the Policy Select Logic circuit 54 generates an Arbitration Policy signal that is connected to an input of Logic Circuit 50. Moyer, at paragraph 0021. Moyer goes on to state:

Bus Arbiter 34 uses **information about a current transfer** to make Global Bus 12 control decisions upon receipt of one or more bus requests to use Global Bus 12. When Logic Circuit 50 receives one or more bus requests from any of CPU 14 and Alternate Bus Masters 36, 38, and 40, a decision is made within Logic Circuit 50 **based upon some predetermined criteria** as to which bus request should be serviced first.

* * * *

Logic Circuit 50 conditionally asserts the Bus Grant CPU signal or a Bus Grant signal for one of the requesting Alternate Bus Masters 36, 38, and 40 **based on the Current Transfer Type Signals 53 and information contained in Control Register 56.** If bus ownership is transferred to a master other than the one performing the current transfer (i.e. transfer master status from a present or current communication bus master), the current transfer is interrupted, and a

previously asserted bus grant signal is negated in order to force the Global Bus 12 to be relinquished and thus allow the higher priority master to gain bus ownership during an on-going burst transfer. Moyer, at paragraph 0022 (emphasis added).

Thus, Moyer discloses a bus arbitration scheme, wherein bus ownership is assigned based upon: (1) information about the transfer currently taking place on the global bus; and (2) some predetermined arbitration policy.

In contrast to Moyer, claim 1 of the present application, as amended herein, recites a method including the following limitations:

1. A method comprising:
initializing a circuit said circuit having at least one memory element coupled to a memory bus on a host system;
monitoring signals on the memory bus;
detecting a first sequence of signals, the first sequence of signals including a **reserved memory address**; and
switching control of the at least one memory element to the circuit in response to detection of the first sequence of signals.

Each of independent claims 11 and 20, as amended, as well as new claim 36, recites some limitations similar to those recited in claim 1 above. The claim amendments proposed herein, as well as new claims 30-43, find support in the as-filed specification at paragraphs 0020 through 0033, notably paragraphs 0023 and 0028-0031.

Thus, the present claimed invention is directed to a scheme wherein a memory bus is monitored for a sequence of signals that includes a reserved memory address. If the reserved memory address is detected on the memory bus, control of a memory is switched from one processing unit to another in response to the detection of this signal

sequence that includes the reserved memory address. The reserved memory address corresponds to an address in a reserved portion of the memory (or another memory). Moyer does not disclose this method of switching control of a memory between two separate processing units.

Accordingly, as Moyer fails to teach at least the above-noted limitations of each of independent claims 1, 11, and 20 (as well as new claim 36), each of these claims is novel in view of Moyer. Also, claims 2-10 (and 30-31), claims 12-19 (and 32-33), and claims 21-29 (and 34-35) are allowable as depending from novel independent claims 1, 11, and 20, respectively.

CONCLUSION

Applicants submit that claims 1-43 are in condition for allowance and respectfully request allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 02-2666.

Respectfully submitted,

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